IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LINEAR TECHNOLOGY CORPORATION Plaintiff, v. MONOLITHIC POWER SYSTEMS, INC. Defendant.	)	C.A. No. 06-476 (GMS)

PLAINTIFF LINEAR TECHNOLOGY CORPORATION'S
ANSWERING CLAIM CONSTRUCTION BRIEF

MORRIS, NICHOLS, ARSHT & TUNNELL LLP
Jack B. Blumenfeld (#1014)
Karen Jacobs Louden (#2881)
James W. Parrett, Jr. (#4292)
1201 N. Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
Attorneys for Plaintiff Linear Technology Corporation

OF COUNSEL:

Raphael V. Lupo
Joel M. Freed
Mark G. Davis
Ronald J. Pabis
Matthew G. Cunningham
McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005
(202) 756-8000

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INTRODUCTION

Plaintiff Linear Technology Corporation ("Linear") submits this brief in response to the opening brief of Defendant Monolithic Power Systems, Inc. ("MPS"). (D.I. 51.)

Contrary to controlling authority, MPS ignores the specification and relies almost exclusively upon dictionary definitions taken out of context. As the Federal Circuit held in *Phillips*, "[t]he specification is … the primary basis for construing the claims." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (*en banc*). The *Phillips* court explained that claim construction is viewed from the perspective of one of ordinary skill in the art. That person is deemed to read the claim terms in the context of the specification, which – may either explicitly or implicitly – provides meaning to the claims. *Id.* at 1313, 1321.

Indeed, the *Phillips* court expressly abandoned the "dictionary-first" rule of claim construction and held that intrinsic evidence is paramount in interpreting claims. *Id.* at 1320-21. Courts may rely "on dictionary definitions when construing claim terms, so long as the dictionary definition *does not contradict* any definition found in or ascertained by a reading of the patent documents." *Id.* at 1322-23 (emphasis added). *See also Free Motion Fitness, Inc. v. Cybex Int'l*, 423 F.3d 1343, 1348-49 (Fed. Cir. 2005) ("The court must ensure that any reliance on dictionaries accords with the intrinsic evidence..."). The Federal Circuit observed in *Phillips* that dictionaries attempt to aggregate all possible definitions for particular words and cautioned that applying all definitions not expressly disclaimed will result in unduly broad claims. 415 F.3d at 1321.

Nevertheless, MPS offers dictionary definitions to support its constructions that are inconsistent with the specification. That approach should be rejected.

MPS's claim constructions also are predicated on fundamental misconceptions of how the patented voltage regulators work, the scope of the Patents-in-Suit, and Linear's

representations to the United States Patent and Trademark Office ("USPTO") during the prosecution of the '178 Patent. For example, MPS incorrectly maintains that the regulator's output (and hence relative thresholds) must be fixed and immutable regardless of circuit design and conditions. MPS also mistakenly suggests that the claimed voltage regulators of the hysteretic comparator embodiment of Fig. 2 would not work if the voltages during the first and second states had the same average value. In addition, MPS frequently mischaracterizes Linear's statements to the Examiner as prosecution disclaimers, when they plainly are not, and has proposed constructions so narrow that they would exclude the preferred embodiments of the Patents-in-Suit.

Finally, without sound basis, MPS disagrees with almost all of the claim constructions reached by the *Impala* district court, and seeks to justify that by criticizing Linear for not adopting the *Impala* claim construction *in toto*. That criticism is misplaced. Linear continues to adhere to the *Impala* claim construction, as modified by the Federal Circuit. Linear has merely corrected a few technical errors in the *Impala* court's constructions for the "first means," "second means," and "third means."

I. CLAIM CONSTRUCTION OF DISPUTED TERMS

A. "Threshold"/"Threshold Fraction Of Maximum Rated Output Current"/"Selected Sleep Mode Current Level"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
threshold (Claim 3 of '258 Patent)	Predetermined level or value at which some change in circuit operation takes place. (Predetermined means determined by design, and includes levels or values that may be fixed or variable.)	A fixed point, such as a current or voltage level, for a given effect, result, or response.
threshold fraction of maximum rated	Predetermined level or value at which some change in circuit operation takes place, wherein that level or value is a	A fixed number greater than zero that is selected as a proportionality of two

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
output current (Claims 1, 34, 41 of '178 Patent)	number greater than zero that represents the proportionality of two positive numbers, the proportion being relative to a rated maximum output current. (Predetermined means determined by design, and includes levels or values that may be fixed or variable.)	numbers, the proportion being relative to maximum rated output current.
selected sleep mode current level (Claim 55 of '178 Patent)	A current level below which the regulator enters into a second mode of operation.	A fixed current level that represents a percentage of maximum rated output current below which the regulator is operated in a second mode of circuit operation.

Properly construed, the "threshold" and "threshold fraction" limitations refer to a level at which some change in circuit operation takes place. This level is predetermined by circuit design, and may be either fixed or variable depending on the type of circuit used as part of the voltage regulator architecture. The "selected sleep mode current level" is a current level below which the regulator enters into a second (*i.e.*, sleep) mode of operation. The language of this term does not include any notion of being fixed. Linear's constructions are consistent with the specification and the scope of the preferred embodiments described in the Patents-in-Suit.

In contrast, MPS's assertion that the "threshold," "threshold fraction," and "current level" limitations should be narrowed to further require that they be "fixed" contradicts both the specification and the Federal Circuit's *Impala* opinion. As detailed in Linear's opening brief (D.I. 52 at 31-35, 38), MPS's attempt to require that the current level that triggers the second state of operation be fixed would exclude at least two of the preferred embodiments. Such a claim interpretation "is rarely, if ever, correct." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1581 (Fed. Cir. 1996).

MPS fails to point to anything in the specification that would support such a strained reading of these claim terms. Instead, MPS cites to a hodgepodge of passages from the specification, which simply point out aspects of some embodiments. For example, MPS cites to a general discussion regarding what constitutes a high load current level, "e.g., greater than 20% of the maximum rated current." '178 Patent (Joint Appx., Tab A) at 6:16-18. The patent makes clear that the 20% example is just that – an example – as exemplified by the use of the term "e.g." The specification also *expressly identifies* other embodiments using other circuits whose outputs (and hence relative threshold levels) vary with changes in input voltage, such as the Constant Off Time (COT) circuit of Fig. 7 and Pulse Width Modulators (PWMs).

For example, the '178 Patent teaches the use of a COT whose output varies with changes in input voltage:

> In accordance with another feature of the present invention, one-shot circuit 25, which provides a constant OFF-time signal, could be replaced with a one-shot circuit that provides a variable OFF time control signal dependent upon the output voltage (V_{OUT}) and the input voltage (V_{IN}).

Id. at 9:23-27. This is consistent with both the embodiment of Fig. 7 (utilizing a COT circuit whose output varies with changes in input voltage) and claim 1 and its dependent claims. Indeed, claim 14 of the '178 Patent, which depends from claims 1 and 7, specifically covers a COT circuit whose output varies with changes in input voltage:

> 14. The circuit of claim 7, wherein second level is generated [by the COT] for a time period dependent upon the input voltage.

Id. at 17:41-43. Because dependent claim 14 covers the use of a COT whose output varies with changes in input voltage (V_{IN}) (*i.e.*, "dependent upon the input voltage"), so must claim 1 from which claim 14 depends. *See Phillips*, 415 F.3d at 1314 ("Other claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of

a claim term."). MPS's attempt to construe the claims as excluding variable output should be rejected.

The specification provides additional examples of circuits whose output varies with changes in the input voltage. For example, it identifies the use of a PWM circuit as part of the voltage regulator architecture. In fact, the '178 Patent identifies PWMs as direct substitutes for COTs:

> As discussed above, the embodiments of the control circuits of the present invention shown in FIGS. 2-4 include one-shot circuit [COT] 25. In accordance with another feature of the present invention, the one-shot circuit could be replaced with other types of circuits that control the duty cycle of the power switch. For example, one-shot circuit [COT] 25 could be replaced with a pulse-width modulated [PWM] signal in response to a control signal.

'178 Patent (Joint Appx., Tab A) at 9:12-22. In fact, MPS acknowledges that the invention encompasses variable output: "Changes in input voltage in a PWM regulator (such as the accused MP1543) can affect the output current level at which both the regulator's switching transistors are simultaneously off." (D.I. 51 at 6.)

The *Impala* district court did note that "[b]ecause the maximum rated output is constant, [it had] difficulty discerning how the threshold fraction of that output could be anything other than a constant percentage." *Impala* Claim Construction Order ("*Impala* CCO") (Joint Appx., Tab N) at N-13. The maximum rated output current, however, is not itself always constant. As shown in the examples cited above (COT of Fig. 7 and PWMs), maximum output current may vary with changes in input voltage.

The specification itself also contains many examples where the word "threshold" describes variable levels. *Id.* at Fig 7; 4:36-41; 6:17-47; and 12:14-29. Given the consistently broad usage of the term "threshold" in the specification to embrace variable levels, MPS's

proposed construction, which would exclude embodiments whose outputs vary with changes in input voltage, should be rejected.

MPS's arguments regarding "selected sleep mode current level" fare no better. As an initial matter, MPS wrongly equates this limitation with the "threshold" limitation despite their different wording. (D.I. 51 at 16.) The *Impala* district court recognized that these two limitations are different and that Linear preserved their distinction throughout the prosecution process. *Impala* CCO (Joint Appx., Tab N) at N-30. It found "selected sleep mode current level" and "threshold fraction" to be different from one another, and declined to equate the two terms. *Id.* This Court should do the same. And regardless of how "threshold" is construed, the "sleep mode" should be construed consistent with the plain language of the term "selected sleep mode level," which lacks any notion of being fixed.

MPS's cites to the '178 Patent file history in an effort to equate the "selected sleep mode current level" and "threshold fraction" limitations also fail. MPS argues that the term "selected sleep mode current level" was added to claim 55 (prosecuted as application claim 97) in a June 5, 1995 Response to Office Action for the same purpose as the claims reciting "threshold fraction," *i.e.*, to more particularly point out the threshold level below which the switching transistors of the claimed regulator are turned off. (D.I. 51 at 14-16.) In fact, the term "selected sleep mode current level" was *not* added – it was already part of a claim appearing in the application long before that 1995 Response.

The passages of the prosecution history that MPS cites to bolster its assertion that terms should be construed as a "fixed" value also do not support its position. (D.I. 51 at 14-16.) In fact, they do not suggest that the threshold level (below which the switching transistors are

concurrently turned off) must remain fixed. Linear pointed to the 20% level as *one example* of an acceptable threshold level:

> When the output current of the regulator drops below a threshold level -- i.e. below some fraction (e.g., 20%) of the regulator's maximum rated output current -- the regulator's switching transistors are turned off simultaneously for a period of time while previously stored energy in the regulator's output circuit supplies current to the load.

June 5, 1995 Response to Office Action (Joint Appx., Tab K) at K-6. *See also* '178 Patent (Joint Appx., Tab A) at 6:16-18. Nowhere in the file history did Linear disclaim the embodiments (*i.e.*, COT circuit of Fig. 7 or PWMs) that require the output voltage (and hence relative threshold level) to vary along with changes in the input voltage.

MPS also relies on dictionary definitions to support its assertion that these claim terms should be "fixed." (D.I. 51 at 12-13.) Dictionary definitions, however, cannot be used to contradict the specification and to read embodiments out of the claims. *Phillips*, 415 F.3d at 1321-1323 ("[H]eavy reliance on the dictionary divorced from the intrinsic evidence risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification."). Rather, "the best source for understanding a technical term is the specification from which it arose." *Id.* at 1315. Because MPS's dictionary definitions would exclude the embodiments described in the specification, they cannot be correct.

MPS next argues that Linear's proposed constructions are wrong because they are "not fixed or selected at all but rather are allowed to fluctuate arbitrarily without limit." (D.I. 51 at 11.) But Linear never proposed that the level at which the voltage regulator circuit goes to sleep is arbitrary or without limit. As the '178 Patent teaches, the third circuit (or third means)

determines when the switching transistors go to sleep.[1] Thus, the "threshold" is *predictably* set by the design of that circuit. Linear therefore has referred in its construction to "predetermined by design." Depending on the particular design of that circuit, the "threshold" can either be fixed or variable. As discussed above, according to the specification, the "threshold" is fixed for the COT circuit of Fig. 2, while it varies (as input voltage varies) for either the COT circuit of Fig. 7 or PWMs. Thus, in two of these three examples disclosed in the specification, the "threshold" for triggering sleep mode varies as *predicted* by the design of the circuit and the range of input voltage applied.

B. "First state Of Circuit Operation"/"Second State Of Circuit Operation"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
first state of circuit operation (Claims 1, 34, 41 of '178 Patent) (Claims 1, 34 of '258 Patent)	A state in which the switching transistors are both enabled for switching and are synchronously switched such that one transistor is ON and the other is OFF, with a varying duty cycle to maintain a regulated voltage at the output terminal.	A state in which the output voltage is maintained during high load current conditions by switching the switching transistors in a complementary manner to provide power to the load.
second state of circuit operation (Claims 1, 34, 41 of '178 Patent) (Claims 1, 34 of '258 Patent)	A state (excluding deadtime) during which both switching transistors are OFF and current is supplied to the load by the output capacitor.	A state in which, as a result of low load current conditions, the output capacitor maintains the output voltage substantially at the regulated voltage, while the switching transistors are disabled.

The "first state of circuit operation" refers to a state where the switching transistors are synchronously switching in a non-overlapping fashion to provide current necessary to maintain a regulated voltage at the output terminal. The "second state of circuit operation" refers to a state

[1] *See e.g.*, '178 Patent (Joint Appx., Tab A), claim 1.

during which both switching transistors are OFF in an effort to conserve power. Linear's proposed constructions comport with the intrinsic evidence.

MPS relies on the ALJ's Initial Determination ("ID") from the '564 Investigation. That reliance is misplaced. The ALJ incorrectly construed a "first state of circuit operation" and "second state of circuit operation" to be strictly linked to high and low load currents, respectively. (D.I. 51 at 19.) That restriction conflicts with the specification, the plain language of the claims, and the prosecution history.

Nothing in the claim language or the specification requires that the first and second states only occur at specific load current levels. The specification describes the first state as *generally* occurring during high and medium load currents and the second state as *generally* occurring during low load currents. It teaches, however, that the circuit may periodically change back and forth between the second and first states *during* extended periods of *low* load current. *See* '178 Patent (Joint Appx., Tab A) at 7:2-5 and 10-16 (in reference to Fig. 2); *id.* at 8:61-9:3 (in reference to Fig. 4); *id.* at 13:14-19 (in reference to Fig. 7). These passages explain that the recharging operation (during low load current) can occur by momentarily going back to the first state of circuit operation (*i.e.*, by alternately turning the switching transistors on and off) during extended periods of *low load current* to recharge the output capacitor C_{OUT}. *Id.* Indeed, if the circuit did not periodically switch back to the first state of circuit operation during extended periods of low load current demand, the capacitor (and also the load) would run out of current.

MPS's attempt to tie the first and second states with particular load current levels thus is misguided. The proper emphasis with the first and second states is on the switching behavior of the transistors. In other words, the crux of defining the first and second states depends on whether the transistors are synchronously switching (first state) or are concurrently OFF (second

state), not on the level of load current demand. The specification spells out how to control the switching behavior of the transistor pair (within a voltage regulator) to achieve high efficiency throughout the entire operating range. *See e.g., id.* at 5:44-7:47 (Fig. 2) and 12:1-14:10 (Fig. 7). MPS's construction contradicts the specification and improperly seeks to read in a limitation that excludes the disclosed embodiments where switching takes place even though the load demand remains low. Accordingly, it must be rejected. *See Vitronics Corp.*, 90 F.3d at 1581 (Claim interpretation that excludes the preferred embodiments "is rarely, if ever, correct.").

MPS's argument that Linear disclaimed the embodiments of the invention that are described in the specification during prosecution also is unfounded. Although the doctrine of prosecution disclaimer precludes patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution, for prosecution disclaimer to apply the "alleged disavowing statements [must be] both so clear as to show reasonable clarity and deliberateness … and so unmistakable as to be unambiguous evidence of disclaimer." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323, 1325 (Fed. Cir. 2003); *see also Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002) (requiring "an intent to deviate from the ordinary and accustomed meaning of a term … by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.").

Linear made no disclaimers – much less the required "unambiguous" and "unmistakable" disclaimers. The prosecution excerpts MPS cites (D.I. 51 at 15-21) relate only to how the second state is *triggered*. The first and second states are nowhere restricted to a particular level of load

current throughout their duration.[2] As Linear explained, its amended language "more particularly recites the relationship between load current and the **turning off the transistors**." July 15, 1994 Response to Office Action (Joint Appx., Tab G) at G-12 (emphasis added). Nothing in that explanation restricts load current levels throughout the states. Indeed, beyond what triggers the second state, Linear made no statements of any kind relating to the level of load current throughout the duration of the first and second states.

There was no restriction of the first and second states of circuit operation to high and low load current conditions, respectively, to overcome the Inam and Josephson references. Rather, Linear pointed out that its invention turns off both switching transistors for efficiency reasons – to *initiate* sleep mode – under low output current conditions, which is precisely the opposite condition (*i.e.*, overcurrents) that requires the transistors of Inam and Josephson to turn off for safety reasons.[3]

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[2] MPS's citation to the prosecution history dealing with turning off both switching transistors – the very act of *initiating* sleep mode – as a function of low load current: "… the invention is based on turning off both switching transistors as a function of the load current." July 15, 1994 Response to Office Action (Joint Appx., Tab G) at G-13; "… improved efficiency during periods of low load current." *Id.* at G-12; "… no teaching in Inam that the circuit turns off both transistors 208 and 212 as a function of the load current." *Id.* at G-14; "… the switching transistors of applicants' regulator are turned off if the current supplied to the load falls below a threshold level." June 5, 1995 Response to Office Action (Joint Appx., Tab K) at K-6 to K-7 (emphasis in original); and "When the output current of the regulator drops below a threshold level … the regulator's switching transistors are turned off simultaneously..." *Id.* at K-6.

[3] '178 Patent prosecution history, July 15, 1994 Response to Office Action (Joint Appx., Tab G) at G-14 ("… Inam … 'comprises circuitry to introduce current limiting and dead time between the switching transistors' (Inam, column 4, lines 19-26).") and '178 Patent prosecution history, June 5, 1995 Response to Office Action (Joint Appx., Tab K) at K-8 ("Josephson teaches current limiting to turn off switching transistors to protect them from overcurrents (Josephson, column 2, lines 28-34).").

C. "First Control signal"/"Second Control Signal"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
first control signal (Claims 1, 34 of '178 Patent) (Claims 1 of '258 Patent)	A control signal generated by the second circuit and used to affect the operation of other circuitry.	A signal generated by the second circuit and used to affect the operation of other circuitry, which signal is separate and distinct from the "second control signal."
second control signal (Claims 1, 34 of '178 Patent) (Claims 1 of '258 Patent)	A control signal generated by the third circuit and used to affect the operation of other circuitry.	A signal generated by the third circuit and used to affect the operation of other circuitry, which signal is separate and distinct from the "first control signal."

The only dispute with respect to the two control signals is whether the "first control signal" and "the second control signal" are "separate and distinct." Although it is not clear what MPS means by "separate and distinct," Linear disagrees with MPS's construction to the extent that MPS seeks to impose a requirement that the first and second control signals cannot use any common pathway and must remain completely isolated. Such a restriction is not supported by the intrinsic evidence.

Nowhere does the specification state or suggest that the first and second control signals must be isolated from, and not pass through any common elements. A person of ordinary skill in the art reading the specification would understand that the first and second control signals are not precluded from sharing anything in common and thereby interacting with one another. To require redundant circuitry just to isolate these two signals would defy common sense, especially given that the ultimate goal of modern electronics is to reduce the footprint of semiconductor devices. MPS's attempt to conflate the issue of the control signals being distinct (*i.e.*, separately identifiable) with that of one signal not being able to affect the other is incorrect.

Although MPS argues that Linear "conflate[s] these two signals into one" and, in effect, reads out a claim limitation (D.I. 51 at 22), to the contrary, Linear recognizes that there are two separately identifiable claim limitations, a first control signal and a second control signal. This is evident from Linear's construction, which takes the *Impala* district court's construction of the generic phrase "control signal"[4] and adds to it the circuit that generates the first or second control signal, respectively. The parties agree that the plain language of the claims requires that the first control signal be generated by the second circuit and that the second control signal be generated by the third circuit. *See e.g.*, '178 Patent (Joint Appx., Tab A), claim 1.

The claim language also provides the context as to why these control signals are separately identifiable. As claim 1 of the '178 Patent states, the first control signal is "responsive to the first feedback signal" and is used "to vary the duty cycle of the switching transistors …" *Id.* On the other hand, the second control signal is used "to cause both switching transistors to be simultaneously OFF for a period of time…" *Id.* That the first and second control signals are separately identifiable from one another does not also mean, however, that these control signals are isolated from and cannot interact with each other.

The cases MPS cites also do not support its position that "separate and distinct" means that the first and second control signals cannot affect, or interact with, one another. (D.I. 51 at 22-23.) In *Bell Atlantic*, the court found that a "first program" and a "second program" recited in the specification for the patent at issue meant "separate programs." That court did not say, however, that "separate" meant "isolated from each other." *See Bell Atl. Network Servs. v. Covad Communs. Group, Inc.*, 262 F.3d 1258, 1271 (Fed. Cir. 2001). Similarly, when the

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[4] The parties each cite the *Impala* district court's construction of "control signal" as "a signal generated by a circuit and used to affect the operation of other circuitry." D.I. 52 at 29; D.I. 51 at 24; Joint Appx., Tab N at N-8.

Rambus district court construed the claim terms "first external clock" and "second external clock" as having "different" timing information, it did not additionally limit the terms by stating that these clock signals could not affect one another. *See Hynix Semiconductor, Inc., v. Rambus, Inc.*, No. CV-00-20905, 2004 U.S. Dist. LEXIS 23230, at * 65-6 (N.D. Cal. 2004). Lastly, MPS's reliance on *Ethicon Endo-Surgery* is inapposite because it is not Linear's position that the first control signal and the second control signal are synonymous. *See Ethicon Endo-Surgery v. United States Surgical Corp.*, 93 F.3d 1572, 1578 (Fed. Cir. 1996).

D. "Third Circuit"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
third circuit (Claim 1 of '178 Patent) (Claims 1, 34 of '258 Patent)	An assembly of electronic components forming a control circuit that is distinct from each of the first and second circuits in that not every electronic component of the circuits is the same.	A circuit that is separate and distinct from both the "first circuit" and "second circuit."

The "third circuit" certainly is distinct from the first and second circuits in that not every electronic component of the three circuits is the same. But that does not foreclose sharing components. As already indicated, miniaturization is a key factor in modern electronics. It would greatly impede that goal to have "separate and distinct" circuitry that does not share a single common component. In permitting sharing, Linear's construction remains consistent with that of the *Impala* district court which held, "[t]he third circuit is distinct from each of the first and second circuits…" Joint Appx., Tab N at N-9. What the claims and specification contemplate is the existence of three identifiable circuits. *See e.g.*, claim 1 of the '178 Patent (Joint Appx., Tab A). They do not foreclose component sharing, however.

To the extent that MPS's proposed construction would foreclose the third circuit from having any common circuit components with the earlier claimed first or second circuits, such a

limitation has no foundation in the specification. MPS has not cited any intrinsic evidence or case law[5] whatsoever to support such a construction. Nor has Linear contended, as MPS suggests, that the circuits can be exactly the same circuits. The third circuit is distinct from the first or second circuits, but that does not mean that the third circuit cannot share some elements or have some overlap with the circuitry of the other circuits. Any construction requiring otherwise would exclude from the scope of the claims the preferred embodiments (such as those of Figs. 2, 3, 7, 9, and 10), which share circuit components between the second and third circuits. Thus, Linear's construction is correct.

E. "Regulated Voltage"/"Substantially At The Regulated Voltage"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
regulated voltage (Claims 1, 34, 41, 55 of '178 Patent) (Claims 1, 34 of '258 Patent)	A voltage having a controlled value.	A predetermined and essentially constant output voltage.
substantially at the regulated voltage (Claim 41 of '178 Patent) (Claims 1, 34 of '258 Patent)	A voltage having a controlled value, and allowing for, but not requiring, greater variation than the regulated voltage (i.e., controlled value).	A voltage that has a different average value than the regulated voltage.

In the sleep mode claims, the voltage is maintained "at the regulated voltage" during the first state of circuit operation and "substantially at the regulated voltage" during the second state of circuit operation. *See, e.g.*, '178 Patent (Joint Appx., Tab A) at 7:6-26, 13:18-20, and 20:5-15; '258 Patent (Joint Appx., Tab B) at 16:40-57 and 19:3-7. MPS's assertions that the "regulated

[5] The cases on which MPS relies in support of its proposed construction of "third circuit" in Section C above are the same cases that MPS uses to support its proposed construction of "first control signal" and "second control signal."

voltage" must be "predetermined" and "constant" and that "substantially at the regulated voltage" excludes "at the regulated voltage" are both incorrect.

The specification uses the phrase "regulated voltage" to mean a controlled value, not a predetermined and essentially constant value. '178 Patent (Joint Appx., Tab A) at 3:53-58; 4:1-3; 6:39-41; 53-58; and 7:6-32. Thus, the *Impala* district court construed "regulated voltage" as "a voltage having a controlled value." Joint Appx., Tab N at N-8. MPS relies on the Background of the Invention to support its construction. That Background, however, does not state or suggest that the invention is restricted to a predetermined and essentially constant voltage. D.I. 52 at 18; '178 Patent (Joint Appx., Tab A) at 1:12-14.

MPS also relies on dictionary definitions to support its position that a regulated voltage is constant. Such dictionary definitions should not be relied on, however, when they contradict the specification. *Phillips,* 415 F.3d 1303, 1321-23. Here, there is no embodiment disclosed in the specification that shows a switching voltage regulator with a constant output voltage. To the contrary, the output voltage varies around and is controlled to be substantially equal to the nominal value V_{REG} set by the reference voltage V_{REF} and the values R1 and R2 of the resistor divider. '178 Patent (Joint Appx., Tab A) at 4:24-30, 4:46-52, 6:61-7:21.

Furthermore, the plain and ordinary meaning of the term "substantially at the regulated voltage" logically encompasses voltages that are near or "at the regulated voltage." The *Impala* district court agreed, concluding that "substantially at" allows for, but does not require, greater variation in the regulated voltage. Joint Appx., Tab N at N-25. Relying on ALJ Harris's unsupported construction, however, MPS proposes a construction of "substantially at the

regulated voltage" that *excludes* operation *at* the regulated voltage. As Linear detailed in its opening brief (D.I. 52 at 20-24), that construction is clearly erroneous for numerous reasons.[6]

In any event, MPS's proposed construction stems from a lack of understanding of fundamental concepts of the subject circuitry. According to MPS, operation at the regulated voltage must be excluded because "[T]he voltage regulators disclosed in the Linear Patents would not work if the two voltages had the same average value." (D.I. 51 at 26.) That is wrong.

Assuming *arguendo* that the claims were limited to the hysteretic comparator embodiment as MPS asserts (which they are not), the *average* value of the output voltage may nevertheless be the *same* in the first and second states. For example, in the preferred embodiments of Figs. 2 and 7, the output voltage in the second state is limited by the upper and lower thresholds of the hysteretic comparator. '178 Patent (Joint Appx., Tab A) at 7:6-17. The upper and lower thresholds are set above and below the nominal regulated voltage level V_{REG}. *Id.* at 6:55-58 and 7:10-15. The amount of variation in the output voltage above and below V_{REG} depends on the comparator's hysteresis, and there is no limit specified for the hysteresis or the thresholds. *Id.* at 6:64-7:5 and 7:15-17. The comparator thresholds can be chosen to correspond to output voltages above and below V_{REG} by the *same* amounts, resulting in an average output voltage in the second state that is the *same* as the average output voltage in the first state.

In other words, if V_{REG} (at the regulated voltage) equals 5.0 volts, and the upper and lower thresholds of the hysteretic comparator (substantially at the regulated voltage) are set at

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[6] The ALJ's construction (1) contradicts well-established Federal Circuit law interpreting the term "substantially," (2) is contrary to the interpretation of the same claim term in the *Impala* litigation, (3) limits the asserted claims to a particular embodiment involving a hysteretic comparator (while explicitly ignoring another embodiment that does not use such a comparator), and (4) violates the doctrine of claim differentiation by impermissibly reading the hysteretic comparator limitation of claim 5 of the '258 Patent into the other preceding claims. (D.I. 52 at 20-24.)

5.3 and 4.7 volts, respectively, by a offset voltage (V_{OS}) of 0.3 volt, then the *average* output voltage in the second state (*i.e.*, average of 5.3 and 4.7 volts = 5.0 volts) is the *same* as the *average* output voltage in the first state (*i.e.*, 5.0 volts). Therefore, even though the *average* output voltage in the second state is the *same* as the *average* output voltage in the first state, this circuit would still operate.

F. "First Means"/"Second Means"/"Third Means"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
a first means for generating a voltage feedback signal indicative of the voltage at the output (Claim 34 of '178 Patent)	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof. The corresponding structures described in the specification include a resistor divider, with or without an operational amplifier, or other conventional voltage feedback circuits.	This is a means-plus-function element governed by § 112 ¶ 6. The structures disclosed in the specification that correspond to the recited function are the following and their equivalents: (i) the combination of resistors 36A and 36B; (ii) the combination of resistors R1 and R2 and operational amplifier 602; and (iii) voltage feedback circuit 220.
a second means for generating a first control signal … to maintain the output terminal at the regulated voltage (Claim 34 of '178 Patent)	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof. The corresponding structures described in the specification include: • As illustrated in Fig. 2, the combination of drive circuit 20, transconductance amplifier 38, offset voltage V_{os} 76, reference voltage 37, current comparator 39, a feedback current path I_{FB} between inductor L_1 32 and current comparator 39, and constant off-time one-shot circuit 25, which outputs the first control signal; • combinations having a pulse-width-modulator circuit or a variable-off-time one-shot circuit	This is a means plus function element governed by § 112 ¶ 6. The structures in the specification that correspond to the recited function are the following and their equivalents: (i) the combination of drive circuit 20, transconductance amplifier 38, offset voltage V_{OS} 76, reference circuit 37, current source I_1 72, current comparator 39, and constant off-time one shot circuit 25, which outputs the first control signal; (ii) combinations having a pulse-width modulator circuit that provides a pulse width modulated signal in response to a control signal, Patent col. 9:18-21; (iii) circuit 240 in Fig. 5.; (iv) the combination illustrated in Fig. 7 (resistors Rsense and R3, one-shot

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
	(*e.g.*, circuit 240 of Fig. 5 or the circuit described at 10:15-16); or • As illustrated in Fig. 7, the combination of resistors R_{SENSE} and R_3, V_{REF}, V_{OS}, current comparator 39, amplifier 38, one-shot circuit 245, off-time controller 250, and capacitor C_{CON}.	circuit 245, off time controller 250 and capacitor C_{CON}); (v) an "operational amplifier," Patent col. 10:15-16; and (vi) the circuitry described at col. 13 lines 36-46.
a third means for generating a second control signal ... the period of time having a duration which is a function of the current supplied to the load by the regulator (Claim 34 of '178 Patent)	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof. The corresponding structures described in the specification include: • As illustrated in Fig. 2, hysteretic comparator 74, V_{REF}, current source I_1 72, and logic circuits 66, 68, and 69; • As illustrated in Fig. 7, combinations such as the circuitry including 72, 74, 315, 316, V_{REF}, and related sleep control logic; or • combinations such as those disclosed at 16:5-12.	This is a means plus function element governed by § 112 ¶ 6. The structures in the specification that correspond to the recited functions are the following and their equivalents: (i) the combination of hysteretic comparator 74, the offset voltage 76, constant current source I_1 (72), logic gates 66, 68, and 69, and reference voltage 37, all as disclosed in Figure 2; and (ii) the circuitry disclosed in Figure 7 (72, 74, V_{OS}, 315, 316 and related sleep control logic).

The parties agree that claim 34 of the '178 Patent is a means-plus-function claim. Thus, under 35 U.S.C. § 112(6), the "first means", "second means", and "third means" of claim 34 must be construed to cover the corresponding structures disclosed in the specification, and equivalents thereof, for carrying out each function. MPS adopts verbatim the *Impala* district court's construction of these terms. (D.I. 51 at 29.) Linear's construction of these terms is consistent with the *Impala* ruling, but corrects certain technical errors contained therein.

MPS nonetheless accuses Linear of proposing constructions inconsistent with its constructions from the previous litigations, and criticizes Linear of having "championed" the

Impala court's construction of this claim in the past, citing to the record of the '564 Investigation for support. *Id.* at 29-30. What MPS fails to recognize is that although Linear did rely on the *Impala* constructions for the claims at issue in the '564 Investigation, it did not assert the '178 Patent there. Thus, claim 34 was not at issue during the '564 Investigation. In any event, there is no inconsistency with Linear's presently proposed construction for claim 34, because it is technically consistent with the *Impala* ruling but more accurately describes the corresponding structures disclosed in the specification.

For example, the *Impala* court's use of "and" between the structures denoted by (i), (ii) and so forth appears to require that all of these structures must be combined to form *one* corresponding structure. This is ambiguous because the elements denoted by (i), (ii) and so forth represent the various corresponding structures disclosed in the specification for each of the "means" recited in the claim.

In addition, the *Impala* court incorrectly included current source (I_1 72 of Fig. 2) as part of the "second means" of this claim. The current source is only part of the third means that causes both switching transistors to be simultaneously OFF during the second state of circuit operation. *See* '178 Patent (Joint Appx. Tab A) at 5:53-58 and 6:47-60. On the other hand, the offset voltage should be included as part of the second means and not the third means, because "[o]ffset V_{OS} 76, which is preferably is built into amplifier 38, level-shifts feedback voltage V_{FB} slightly below reference voltage V_{REF}," thus keeping the circuit in the first state of operation. *See* '178 Patent (Joint Appx. Tab A) at 6:21-25. An offset is used to create a difference between two equal values. To create this difference, an offset need only affect one of these two equal values. It is simply redundant to affect both numbers by the same offset in different directions to

create this difference. Therefore, MPS's inclusion of the V_{OS} 76 as part of *both* the second *and* third means is incorrect.

Linear's construction more accurately describes the corresponding structures disclosed in the specification. Linear's intrinsic support for the corrected "first means" can be found, for example, at '178 Patent (Joint Appx., Tab A), at 4:19-24; 6:19-25; 9:39-45; 12:19-25; resistors R1 and R2; operational amplifier 602; voltage feedback circuit 220; Fig. 2; Fig. 5; and Fig. 7. The intrinsic support for the corrected "second means" can be found, for example, at '178 Patent (Joint Appx., Tab A), at 4:8-52; 5:59-6:6; 6:25-33; 6:61-7:5; 8:1-16; 9:12-22; 10:11-16; 12:1-13:19; 13:40-46; 15:22-35; 15:66-16:4; and output of one-shot circuit 245 in Fig. 7, and the intrinsic support for the "third means" can be found, for example, at '178 Patent (Joint Appx., Tab A), at 6:34-7:5; 12:46-13:2; and 16:5-16; Fig. 2; and Fig. 7.

G. "Switching Voltage Regulator"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
switching voltage regulator (Claims 1, 34, 41, 55 of '178 Patent) (Claims 1, 34 of '258 Patent)	A device or circuit that receives an input voltage and provides a predetermined and regulated output voltage by controlling the opening and closing of one or more switching transistors. (Predetermined means determined by design, and includes voltages that may be fixed or variable).	A device or circuit that is capable of receiving a poorly-specified and fluctuating input voltage and that provides a predetermined and essentially constant output voltage by controlling the opening and closing of a switch.

Utilizing one or more switching transistors, a "switching voltage regulator" provides a predetermined and regulated output voltage from an input voltage. Linear's construction of "switching voltage regulator" is consistent with both the understanding of one of ordinary skill in the art and with the *Impala* construction. MPS offers a litigation-induced construction in which only an idealized regulator – divorced from real-life – could actually infringe the Patents-in-Suit.

First, MPS seeks to add a limitation in which the "switching voltage regulator" can only receive "a poorly-specified and fluctuating input voltage." MPS lifts this language from the Background of the Invention section of the Patents-in-Suit where certain prior art voltage regulators are described. '178 Patent (Joint Appx., Tab A) at 1:6-14. The Background in no way states or suggests, however, that the invention is limited to regulators that use power sources that are not "poorly specified" or do not fluctuate over even a few cycles.

MPS also includes the word "constant" in its proposed construction in an attempt to limit the scope of the asserted claims to switching voltage regulators that only operate under fixed and immutable operating conditions that can never vary. This limitation is contrary to both the intrinsic evidence and the understanding of one of ordinary skill in the art. For example, in describing the invention, the specification speaks repeatedly of how the regulator operates to "maintain the output voltage substantially at the regulated voltage level." '178 Patent (Joint Appx., Tab A) at 7:6-10, *see also id.* at 7:14-16 ("Therefore, V_{OUT} will oscillate between upper and lower thresholds"); *id.* at 8:10-12 ("the output voltage V_{OUT} is able to be maintained substantially a the regulated voltage level V_{REG}"); *id.* at 8:43-44 ("maintain the output voltage V_{OUT} substantially at the output voltage").

As described above for the "threshold" and "threshold fraction" limitations, the specification expressly identifies the use of other circuits whose outputs vary with changes in input voltage, such as the COT circuit of Fig. 7 and PWMs. Therefore, the use of these types of circuits whose outputs vary with changes in input voltage (V_{IN}) must remain within the scope of the claims. MPS's proposed construction for "switching voltage regulator," which would exclude such coverage, should be rejected.

Linear's construction does not call for arbitrary fluctuations in output voltage, as MPS contends, but instead allows variations *predictably* set by the design of a particular circuit. This is what Linear means by "predetermined by design" and depending on the particular design of that circuit, the "output voltage" can either be fixed (COT of Fig. 2) or variable (COT of Fig. 7 and PWMs).

H. "A Pair Of Synchronously Switched Switching Transistors"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
a pair of synchronously switched switching transistors (Claims 1, 34, 41, 55 of '178 Patent) (Claims 1, 34 of '258 Patent)	Two switching transistors are synchronously switched when they are driven out of phase (i.e., one is ON and the other is OFF, except for deadtime) to supply current at a regulated voltage to a load.	A pair of switching transistors are "synchronously switched" when they are "driven out of phase to supply current at a regulated voltage to a load." "driven out of phase" means that the two switching transistors do not turn "on" and "off" at the same time at all times.

Two switching transistors are "synchronously switched" when they are driven out of phase, such that one is ON and the other is OFF except for deadtime, to supply current at a regulated voltage. In particular, when the transistors are synchronously switching in the first state of operation, one transistor is ON while the other is OFF. As the specification explains, the circuit will account for "dead-time"[7] during the first state, so that both transistors are never ON at the same time, to avoid the undesirable "shoot through" effect. '178 Patent (Joint Appx., Tab A) at 5:33-43.

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[7] MPS argues that because Linear has not offered a dictionary definition or shown that these two terms are related, then "dead-time" cannot fall within the construction of "driven out of phase." (D.I. 51 at 34.) It is an elementary tenet of claim construction, however, that dictionary definitions are not the starting point; rather it is "the specification [that] is the single best guide to the meaning of a disputed term." *Phillips,* 415 F.3d at 1321. As explained above, a person of ordinary skill in the art reading the specification would understand that "dead-time" does modify "driven out of phase."

MPS proposes that "driven out of phrase" should be construed to encompass all pairs of switching transistors if there is ever a situation where one is off and the other is on, *i.e.*, if they do not always turn "on" and "off" at the same time. (D.I. 51 at 32.) In other words, MPS contends that every pair of switching transistors is "synchronously switched" as long as the two switches are not perfectly in-phase with one another (*i.e.*, "do not turn 'on' and 'off' at the same time at all times). Under this construction, both switching transistors could be, for example, concurrently ON for 95% of a switching cycle, and still be considered "driven out of phase," as long as the two transistors are out of phase for the remaining 5% of the time. This makes no sense. If the two switching transistors are both concurrently ON for 95% of a switching cycle, enormous amounts of power would be wasted (caused by the short circuit). Moreover, the circuit could be severely damaged by "shoot through" effects. The specification unequivocally teaches away from such deleterious operation. '178 Patent (Joint Appx., Tab A) at 5:33-43. Such a circuit would not even be a voltage regulator; it would serve no useful purpose.

To support its upside-down construction, MPS once again relies on a dictionary definition. (D.I. 51 at 33.) Such definitions cannot be used to contradict the specification, however. *Phillips,* 415 F.3d at 1321-23 (Courts may rely "on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents.").

MPS also argues that Linear's construction excludes all of the preferred embodiments. (D.I. 51 at 33-34.) Not so. MPS asserts that "synchronously switched" recited in the preamble governs the circuit's operation *at all times* despite the different states of circuit operation specifically recited in the body of the claims. MPS also says that the sleep mode of operation is excluded by Linear's proposed construction for "a pair of synchronously switched switching

transistors" because, in that mode, the transistors are no longer synchronously switching. *Id.* MPS is incorrect.

The reference to "synchronously switched" in the preamble does not limit the status of circuit operations specifically recited in the body of the claims. Rather the disputed term appears in the preamble as part of the phrase "a switch … **including** a pair of synchronously switched switching transistors," and does not foreclose the possibility that this pair of switching transistors may be OFF for the second state of circuit operation, as the claims recite. The presence of the word "including" in the asserted claims requires that the circuit (or method) be comprised of switching transistors that are synchronously switched at least some of the time, and may additionally include other times when the same switching transistors are concurrently turned off. In short, the preamble provides the context of how the switching transistors are configured and what they are capable of performing under a given set of conditions. They do not require the transistors to be synchronously switched at all times regardless of the circuit conditions.

Nothing in the claim language or the specification requires that the "pair of synchronously switched switching transistors" must be "synchronously switched" at all times. MPS simply ignores the word "including." The claim language specifically recites, and Linear's construction (by incorporating the concept of "including") clearly recognizes that "both switching transistors" are OFF during the second state of circuit operation.[8] As a result, MPS cannot argue that the operational characteristics of the switching transistors from the first state of

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[8] Among the asserted claims that are independent: claims 1 and 34 of the '178 Patent and claim 1 of the '258 Patent recite "cause both switching transistors … to be simultaneously OFF"; claim 41 of the '178 Patent recites "turning both switching transistors simultaneously OFF"; claim 34 of the '258 Patent recites "turning both switching transistors OFF"; and claim 55 of the '178 Patent recites "prevent … turning on either of the pair of synchronously switched switching transistors." Joint Appx., Tabs A & B.

circuit operation must govern the "pair of synchronously switched switching transistors" of the preamble.

I. "Coupled"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
coupled (Claims 1, 34, 41, 55 of '178 Patent) (Claims 1, 34 of '258 Patent)	Circuit elements are coupled when a current path exists between them.	Circuit elements are "coupled" when they are so arranged that energy can transfer electrically or magnetically from one to another.

Linear submits that circuit elements are coupled when a current path exists between them. In no less than eleven instances, the word "coupled" is used in the specification as calling for a wired current path connection. [10] '178 Patent (Joint Appx., Tab A) at 15:40-46. In no instance is the term "coupled" used to embrace magnetic or inductive energy transfer.

In an effort to set up its invalidity case, MPS nevertheless asserts that the term "coupled" embraces magnetic/inductive energy transfer. That is wrong. Nowhere in the patents or file histories is the term "coupled" used to embrace magnetic/inductive energy transfer. Although MPS asserts that Linear is attempting to narrow the claims to only cover the preferred embodiments, all embodiments use a wired current path connection, not just the preferred embodiment.

Because MPS cannot cite any intrinsic evidence to support its position, it once again resorts to dictionary definitions to contradict the teachings of the specification. (D.I. 51 at 35.) One of ordinary skill in the art, however, would ascertain that "coupled" only refers to a wired

[10] '178 Patent, (Joint Appx., Tab A) at col. 1:17-18; 1:20-22; 3:56-58; 6:43-44; 8:39-40; 8:44-46; 9:50-51; 10:30-32; 12:34-35; 12:44-45; 13:47.

current path connection in view of the Patents-in-Suit (*See e.g.*, '178 Patent (Joint Appx., Tab A) at 1:17-24), MPS's reliance on dictionary definitions that contradict the specification by expanding "coupled" to embrace other types of energy transfer is improper. *Phillips,* 415 F.3d at 1315, 1321-1323.

In a further effort to stretch the meaning of "coupled" to include magnetic/inductive coupling, MPS relies on inapposite case law. In *Liebel-Flarsheim*, the patentee had amended the asserted claims to omit a particular limitation that had previously been present, thereby purposefully broadening the claims during prosecution. *Liebel-Flarsheim Co. v. Medrad, Inc.,* 358 F.3d 898, 911 (Fed. Cir. 2004). The court did not permit the patentee to recapture a limitation that it previously deleted from the claim during prosecution. *Id.* Here, Linear never amended its claims to delete a previously-present limitation; the claims from the beginning never encompassed magnetic or inductive coupling.

MPS's reliance on the construction of "coupled" in *Tegal* also is improper. The court's analysis confirms the importance of the intrinsic evidence to claim construction. The Federal Circuit accepted the district court's construction of the term "coupled" because the litigants had not disputed the district court's construction of that term. *Tegal Corp. v. Tokyo Electron America, Inc.,* 257 F.3d 1331, 1342 n.6 (Fed. Cir. 2001). The district court in *Tegal* granted the plaintiff's proposed construction of "coupled" because it was "*amply* supported by intrinsic evidence ..." *Tegal Corp. v. Tokyo Electron Ltd.*, 1999 U.S. Dist. LEXIS 23348, *26 (E.D. Va. 1999). (emphasis added). Thus, the court in that case found support in the specification of the patent in suit to construe "coupled" to include "inductive" (*i.e.*, magnetic) energy. Here, in contrast, "coupled" should not include magnetic/inductive coupling because there is no support in the intrinsic evidence for such a construction.

Finally, MPS's reliance on *Glaxo* to resort to "an accepted scientific meaning" also is unavailing. *Glaxo Wellcome Inc. v. Andrx Pharms., Inc.*, 344 F.3d 1266 (Fed. Cir. 2003). In another case, similar to this one, a party cited *Glaxo,* arguing that there was no basis to exclude a particular type of limitation (*e.g.*, magnetic coupling) from the disputed term because neither the specification nor the claim limited it to another particular type of limitation (*e.g.*, wired current path connection). *Ranbaxy Labs., Ltd. v. Abbott Labs.*, 2005 U.S. Dist. LEXIS 27753, *37 n.11 (D. Ill. 2005). The *Ranbaxy* court distinguished *Glaxo* because it did not involve a patent whose specification discussed the preferred qualities for the disputed limitation. That reasoning is even more compelling here, because the specification consistently uses the term "coupled" to refer to a wired current path connection.

J. "Load"/"Output Terminal"

CLAIM TERMS	LINEAR'S PROPOSED CONSTRUCTION	MPS'S PROPOSED CONSTRUCTION
output terminal (Claims 1, 34, 41, 55 of '178 Patent)	A point or node of the switching regulator to which the load is coupled.	A specific point of the switching voltage regulator that is directly connected to the load.
load (Claims 1, 34, 41, 55 of '178 Patent) (Claims 1, 34 of '258 Patent)	A device, circuit, or system coupled to the output terminal to which the regulator can supply current.	A device, circuit, or system that consumes electric power; not part of the regulator structure.

Linear relies on the *Impala* district court's construction of "load" and "output terminal." Those constructions are supported by the specification. As explained in Linear's opening brief (D.I. 52 at 15-17), the *Impala* district court did not require that the "load" consume electric power. Also, that court, in construing "output terminal," expressly rejected the "directly connected" limitation that MPS now seeks to add. *Id.* at 15. MPS, on other hand, proposes constructions that do not follow the prior *Impala* constructions and ignore the intrinsic evidence.

MPS once again relies on the Background of the Invention of the '178 Patent, dictionary definitions, and even the Background Section of the Federal Circuit's *Impala* decision to support its position that the load must consume electric power. (D.I. 51 at 36-37.) The Background of the Invention of the '178 Patent only addresses certain voltage regulators, however, not all of the embodiments detailed in the specification.

Second, the dictionary definitions on which MPS relies contradict the specification, which teaches that power can be pulled *from* the load. *See e.g.*, '178 Patent (Joint Appx., Tab A) at. 5:21-23 ("At low output currents this can cause the current in inductor L1 to reverse polarity and, thus, pull power from the load.").

Moreover, the requirement that a load consume electric power can only be met if current is supplied to it by the regulator and the load is configured to consume power. If the regulator runs out of power (*e.g.*, battery completely drained) or the load's power requirement is shut off (*e.g.*, by turning off a switch in the load), it would still be "a device, circuit, or system coupled to the output terminal," but it would not consume electric power. Thus, MPS's proposed limitation should be rejected because under that construction, none of the claims would read on any of the embodiments in the specification. *See Vitronics Corp.*, 90 F.3d at 1581 (Claim interpretation that excludes the preferred embodiments "is rarely, if ever, correct.").

Third, in citing the Federal Circuit's *Impala* decision, MPS asserts that the Federal Circuit construed "load" and amended the district court's construction. (D.I. 51 at 36.) That never happened. The Federal Circuit left this construction undisturbed. *See generally, Linear Technology Corp. v. Impala Linear*, 379 F.3d 1311 (Fed. Cir. 2004) (Joint Appx., Tab P).

MPS's proposed construction for "output terminal" is similarly flawed. Although MPS proposes that the "output terminal" is a "*specific point* of the switching voltage regulator that is

directly connected to the load," it is unclear what the "specific point" is to which MPS or where it is located, as MPS has not defined the physical components that make up the load. For example, there are a number of circuit elements (*e.g.*, filter or switch) that can be placed between the switching voltage regulator and the load. In such a configuration, the output terminal would not be "directly connected" to the load. But nothing in the claims or the specification limits the output terminal to be "directly connected" to the load. MPS seeks to add such a limitation nonetheless in an effort to set up its non-infringement case.

MPS's attacks on Linear's proposed constructions of "load" and "output terminal" as being broad and meaningless are unsound. Deliberately ignoring the words of the claims surrounding the terms "load" and "output terminal," MPS argues that the definition of "coupled" would lead to the existence of multiple loads and multiple output terminals. This is not incorrect. The "load" and "output terminal" must be "coupled" as defined by the claim language: "output terminal … for supplying current at a regulated voltage to a load…" '178 Patent (Joint Appx., Tab A), claims 1, 41, and 55. Because this particular "coupling" requires that the "output terminal" *supply current at a regulated voltage* to the "load," each of the random circuit elements and nodes that MPS characterizes as a potential load or output terminal simply does not fit the criteria. In other words, those random circuit elements and nodes cannot be considered a "load" or "output terminal" given the plain language of the claims. For these reasons, MPS's "load" and "output terminal" constructions should be rejected.

CONCLUSION

For the foregoing reasons, Linear respectfully requests that the Court adopt Linear's proposed construction of the disputed claim terms.

MORRIS, NICHOLS, ARSHT & TUNNELL LLP

/s/ Karen Jacobs Louden

Jack B. Blumenfeld (#1014)
Karen Jacobs Louden (#2881)
James W. Parrett, Jr. (#4292)
1201 N. Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
Attorneys for Plaintiff Linear Technology Corporation

OF COUNSEL:

Raphael V. Lupo
Joel M. Freed
Mark G. Davis
Ronald J. Pabis
Matthew G. Cunningham
McDERMOTT WILL & EMERY LLP
600 13th Street, N.W.
Washington, DC 20005
(202) 756-8000

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CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on June 26, 2007 I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Richard L. Horwitz
POTTER ANDERSON & CORROON LLP

I also certify that copies were caused to be served on June 26, 2007 upon the following in the manner indicated:

BY HAND & EMAIL

Richard L. Horwitz
Potter Anderson & Corroon LLP
1313 N. Market Street
P.O. Box 951
Wilmington, DE 19899

BY EMAIL

Dean G. Dunlavey
Mark A. Flagel
Robert Steinberg
Sean Pak
Latham & Watkins LLP
633 West Fifth Street, Ste. 400
Los Angeles, CA 90017

Mark Kachner
Latham & Watkins LLP
650 Town Center Drive
20th Floor
Costa Mesa, CA 92626-1925

David McKone
Latham & Watkins
Sears Tower, Suite 5800
233 South Wacker Drive
Chicago IL 60606

/s/ Karen Jacobs Louden

Karen Jacobs Louden
klouden@mnat.com